REMARKS

This amendment is filed in furtherance of the Request for Continued Examination that was mailed March 29, 2006. Consideration of both the Request and this amendment is respectfully requested.

Interview Summary

The Examiner is thanked for the interview on May 2, 2006. The difference between the independent claims and the references were discussed. However, no agreement was reached.

Claim Amendments

Claim 1, as amended, relates to a multi-layered printed circuit board and a method for manufacturing without the application of plating and plugging of the circuit layers with paste. This is exemplified by the step "connecting the insulating layers to the circuit layers, wherein the conductive paste filling the via holes of the insulating layers flows into the via holes of the circuit layers by pressing the arranged circuit and insulating layers." The advantage of Claim 1 over the conventional multi-layer printed circuit board is reduced production cost and time due to the omitted plating and plugging steps of the circuit layers.

A conventional multi-layer printed circuit board is described in the application specification, which is manufactured under the condition that circuit patterns are formed prior to the pressing step.

The cited reference, U.S. Patent Application Publication No. 2004-194303, does not disclose a process that includes, at least, the step "connecting the insulating layers to the circuit layers, wherein the conductive paste filling the via holes of the insulating layers flows into the via holes of the circuit layers by pressing the arranged circuit and insulating layers." Furthermore, the cited reference describes pressing the board under the condition that circuit patterns are formed prior to the pressing step, which is different from Claim 1.

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The Examiner regards Claim 1 cannot be patentable by quoting from the cited reference "the plugging process of the via holes 204 using the paste 206 may be omitted in accordance with a purpose of the multilayered PCB" (Para.[0061].) However, the passage does not mean that the via holes of the circuit layers are empty. It means that the via holes of the circuit layers are plugged by plating instead of conductive paste, as is shown in FIGURE 3. Furthermore, the present specification describes that plating and paste-plugging steps for filling via holes of the circuit layers are omitted. (Page 11, lines 5-12.)

CONCLUSION

In view of the foregoing amendment, and the remarks herein and in the paper mailed on March 29, 2006, applicants respectfully submit that Claims 1-10, and 14-17 are allowable. If the Examiner has any further questions or comments, the Examiner is invited to contact applicants' attorney at the number below.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service in a sealed envelope as first class mail with postage thereon fully prepaid and addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the below date.

Date: May 10, 2006

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